Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Atty. Docket No. NVIDP234/P000825	Application No.: 10/633,004
	Applicant: Singh et al.	
	Filing Date: 7/31/2003	Group Art Unit: ~~Unassigned~~ 2811

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						
	L						
	M						
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	Q						
	R						
	S						
	T						
	U						

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
VL	V	Chou, Kuo-Yu et al., "Active Circuits Under Wire Bonding I/O Pads in 0.13 µm Eight-Level Cu Metal, FSG Low-K Inter-Metal Dielectric CMOS Technology +", October 2001, IEEE
VL	W	Efland, T., et al., "LeadFrameOnChip offers Integrated Power Bus and Bond over Active Circuit", 2001, International Symposium on Power Semiconductor Devices & ICs, Osaka
VL		Heinen, Gail et al., "Wire Bonds Over Active Circuits", 1994 IEEE
Examiner	HUNG VU	Date Considered 07/07/05

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	Group Art Unit: ~~Unassigned~~ 2811
Singh et al.	Examiner: ~~Unassigned~~ H. Vu
Application No. 10/633,004	Atty. Docket No. NVIDP234/ P000825
Filed: 7/31/2003	
For: PAD OVER ACTIVE CIRCUIT SYSTEM AND METHOD WITH MESHED SUPPORT STRUCTURE	Date: November 6, 2003

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450 on November 6, 2003.

Signed: Erica L. Farlow

Erica L. Farlow

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §§1.56 AND 1.97(b)

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Vu Application 10/633,021, filed 07/31/2003, may be material to examination of the above-identified patent application. Applicants identify this application in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make this statement an official record in this application. However, IT IS RESPECTFULLY REQUESTED THAT THE APPLICATION SERIAL NUMBER AND FILING DATE NOT BE IDENTIFIED ON ANY PATENT ISSUED FROM THE ABOVE-IDENTIFIED APPLICATION under MPEP §609C(2) and §609D.

HUNG VU 07/07/05

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is believed to be filed before the mailing date of a first Office Action on the merits. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 50-1351 (Order No. NVIDP234/P000825).

Respectfully submitted,
Silicon Valley IP Group, PC

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